# VIRTUAL PLATFORMS FOR THE ORCA CHIP ARCHITECTURE: TWO PERSPECTIVES

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## 1. MOTIVATION

- Memristor-CMOS chip for demonstration of bio-inspired paradigms
- Uses multiple hardware accelerators (Compute Arrays / CAs) based on memristive crossbar arrays (MCBAs) for analog vector-matrix multiplication
- Processing Elements (PEs) are interconnected via a Network on Chip (NoC)

→ **Complex design, internal data transfers, and state management**

- Increasingly difficult to achieve a functional and well-designed system

→ **ICA and ICE create simulations to:**

- Identify optimized components and designs for the system
- Verify the feasibility of the design with regard to the specific application
- Simulators built with top-down and bottom-up approaches respectively

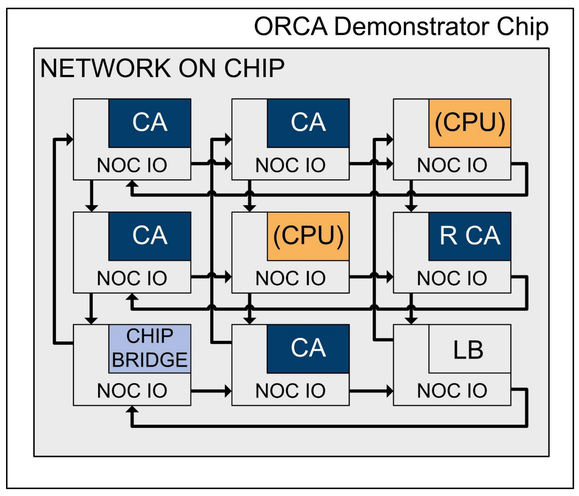


**Fig. 1:** Modular Processing Elements of the NEUROTEC II – ORCA demonstrator chip. Orange CPUs are only present in simulations.

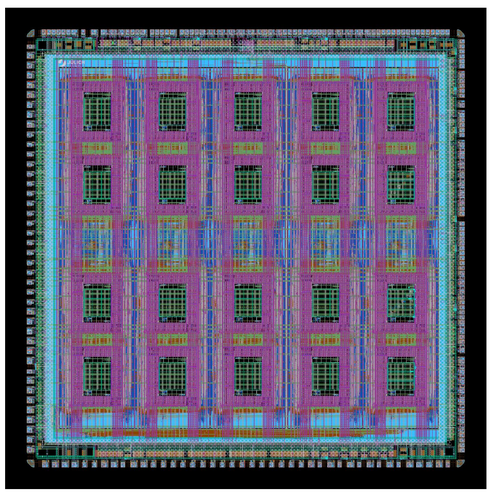

**Fig. 2:** Layout (6 mm × 6 mm) of the NEUROTEC II – ORCA chip in 28nm CMOS technology.

## 2. DESIGN SPACE EXPLORATION IN SYSTEMC

- At **ICE**, a full **SystemC**-based virtual platform, *NeuroVP*[1] in Fig. 3, has been developed to assemble the architecture planned for the ORCA chip
- Components are created from scratch in modules, allowing for flexibility and early design space exploration (DSE)

→ **Goals:**

- Allow for early simulation using NeuroVP of ANN applications expected to run on the actual hardware after tape-out
- Use simulation primarily to forecast performance of the ORCA demonstrator chip in desired applications

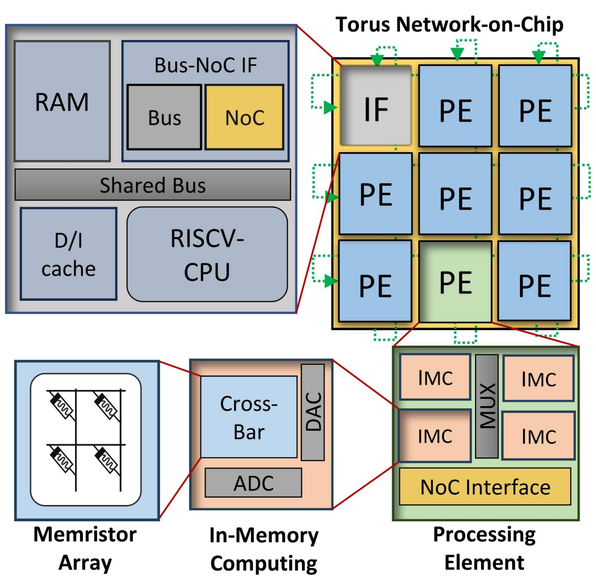


**Fig. 3:** NeuroVP. DSE architecture containing a RISC-V CPU, a Network on Chip and an in-memory computing accelerator based on memristor arrays.

**Methodology:**

- Energy estimations based on consumption of individual components per instruction, as reported in literature
- Performance estimation is based on transaction count

**Results:**

- Early results show some traffic bottlenecks caused by the implemented Network on Chip
- Overall application itself is functional and correct

## 3. SYSTEM VERIFICATION WITH GEM5

- Simulation from **ICA** based on the modular system-level simulator **gem5**
- Components defined in C++, System Architecture and Simulation in Python
- Recreation of the modular ORCA chip using predefined and custom gem5 components, including:
  - Compute Arrays (CAs), Algorithmic Logic Units (ALUs), etc.
  - CPU-PEs based on RISC-V 64-bit architecture and CVA6 CPU (Fig. 4)

→ **Goal:** Verification of hardware design as closely as feasible to specification

→ Verifications include:

- Memory layout and compilation of RISC-V firmware
- Access to the network on chip for each Processing Element
- Suitable data widths of interfaces and transferred data
- Internal state management within CAs, Network Interfaces, etc.

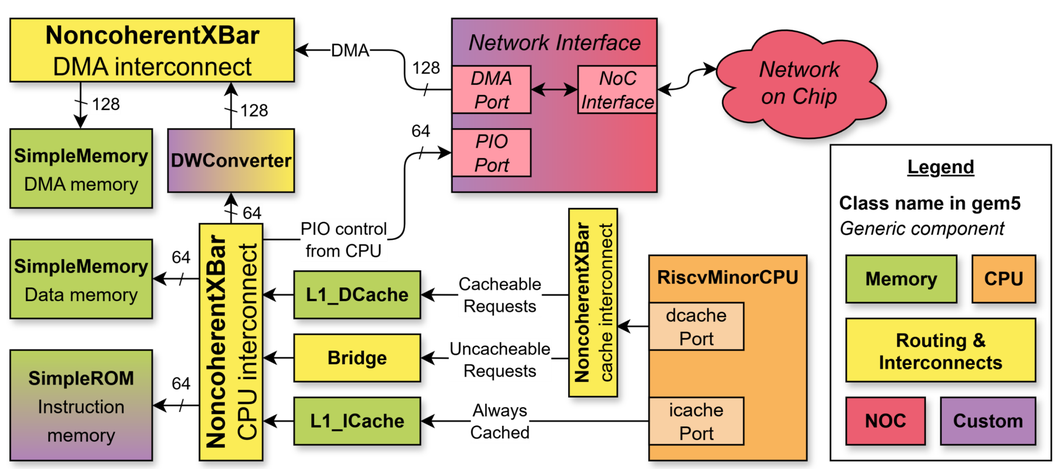


**Fig. 4:** RISC-V CPU simulated in gem5, based on the design of ORCA's processing elements.[2]

## 4. CONCLUSION

- Two simulations of the ORCA chip implemented in **SystemC** and **gem5**
- Useful for design space exploration and system architecture verification

→ Multiple design **improvements already identified and implemented**

→ Build the basis for early design exploration of **future demonstrator chips**

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[1] M. Galicia et al., "NeuroVP: A System-Level Virtual Platform for Integration of Neuromorphic Accelerators", 2021 IEEE 34th International System-on-Chip Conference (SOCC), Las Vegas, NV, USA, 2021
[2] Image based on: Daniel Keßel, "System-Level Simulation of Neuromorphic Hardware Accelerators in gem5", Master Thesis, RWTH Aachen University